Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **GND**
2. **INPUT +**
3. **INPUT +**
4. **V –**
5. **BAL**
6. **BAL/STROBE**
7. **OUTPUT V +**

**.036”**

**13 12 11 10**

**9**

**8**

**7**

**14**

**15**

**16**

**1**

**2 3 4 5 6**

**.039”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .036” X .039” DATE: 5/24/21**

**MFG: MOTOROLA THICKNESS .015” P/N: MC10H105**

**DG 10.1.2**

#### Rev B, 7/1